AMENDMENTS TO THE CLAIMS

1. (Currently amended) A computer system, comprising:

a host processor, including resources supporting a full power mode, a lower power mode and a power down mode; and

a network interface coupled to the host processor via a bus, and coupled to a network, the network interface comprising:

a memory that stores data packets in transit between the host processor and the network;

a medium interface unit coupled to network media supporting at least a high speed protocol and a lower speed protocol;

~~a voltage detector for detecting power supply voltage on the bus; and~~

power management logic comprising a state machine having a full power state, a low power state, and a power down state, configured to cause ~~which forces~~ the medium interface unit to renegotiate from the high speed protocol to the lower speed protocol in response to an event ~~detected by the voltage detector~~ signaling entry of said lower power mode, and to enter a power down state in the event that the lower speed protocol is not successfully negotiated.

2. (Previously Presented) The computer system of claim 1, wherein the network interface in said lower power mode consumes less than a specified power when executing said lower speed protocol, and consumes greater than the specified power when executing said high speed protocol.

3. (Original) The computer system of claim 1, wherein the network interface in said lower power mode consumes less than a specified power of about 1.3 Watts, and the network interface requires greater than the specified power to support said high speed protocol.

4. (Original) The computer system of claim 1, wherein the network interface includes logic operating in the lower power mode using the lower speed protocol to detect a pattern in incoming packets, and in response to detection of said pattern, to issue a reset signal to the host processor.

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5. (Original) The computer system of claim 1, wherein the medium interface unit comprises circuitry for formatting packets according to protocols compliant with 10 Megabit, 100 Megabit and Gigabit Ethernet protocol standards, and wherein said high speed protocol is Gigabit Ethernet, and said lower speed protocol is one of 10 Megabit Ethernet and 100 megabit Ethernet.

6. (Original) The computer system of claim 1, wherein the medium interface unit comprises circuitry for formatting packets according to a protocol compliant with an InfiniBand protocol standard, and wherein said high speed protocol is InfiniBand.

7. (Original) The computer system of claim 1, wherein said host processor monitors the network interface for a wake up event involving a loss of link or a change of link on the network interface, and wherein said power management logic blocks signals indicating said wake up event for a time interval during which the power management logic circuitry forces the medium interface unit to the lower speed protocol.

8. (Currently amended) The computer system of claim 1, wherein said event ~~detected by the voltage detector~~ signaling lower power mode is a signal generated by the host processor.

9. (Currently amended) The computer system of claim 1, wherein the system bus has a full power mode, a lower power mode, and a power down mode, and said event ~~detected by the voltage detector~~ signaling lower power mode comprises a loss of power on the system bus.

10. (Currently Amended) In a network interface apparatus coupled to a bus system having a full power mode, a lower power mode and a power off mode, and supporting a plurality of protocols including a high speed protocol and a lower speed protocol, a method of power management, comprising:

receiving a command at a state machine indicating a sleep state is desired;

sending control signals from the state machine to a medium interface unit to initiate negotiation of a low speed protocol from a high speed protocol;

suppressing a link-change signal at a wake-up detector; and,

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entering a sleep state at the state machine where the network interface operates in a low power mode.

~~forcing the apparatus to execute the lower speed protocol from the high speed protocol upon transition from the full power mode to the lower power mode in response to detecting a voltage change on the bus system.~~

11. (Previously presented) The method of claim 10, wherein the network interface apparatus consumes less than a specified power for said lower power mode when executing said lower speed protocol, and consumers greater than the specified power when executing said high speed protocol.

12. (Original) The method of claim 10, wherein the network interface apparatus consumes less than a specified power of about 1.3 Watts for said lower power mode when executing said lower speed protocol, and consumes greater than the specified power when executing said high speed protocol.

13. (Original) The method of claim 10, including using the lower speed protocol in the lower power mode to detect a pattern in incoming packets, and in response to detection of said pattern, to issue a reset signal to a host processor.

14. (Original) The method of claim 10, including providing resources on the network interface apparatus for formatting packets according to protocols compliant with 10 Megabit, 100 Megabit and Gigabit Ethernet protocol standards, and wherein said high speed protocol is Gigabit Ethernet, and said lower speed protocol is one of 10 Megabit Ethernet and 100 megabit Ethernet.

15. (Original) The method of claim 10, including providing resources on the network interface apparatus for formatting packets according to a protocol compliant with an InfiniBand protocol standard, and wherein said higher speed protocol is InfiniBand.

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16. (Original) The method of claim 10, wherein said host processor monitors the network interface for a wake up event involving a loss of link or a change of link on the network interface, and including blocking signals indicating said wake up event for a time interval while forcing the apparatus to change to the lower speed protocol.

17. (Previously presented) The method of claim 10, further comprising causing transition from the full power mode to the lower power mode in response to a signal generated by a processor.

18. (Previously presented) The method of claim 10, further comprising causing transition from the full power mode to the lower power mode in response to a loss of power on the bus system.

19. (Currently amended) An integrated circuit for use in a network interface between a host processor and a network, the host processor including system bus having a full power mode, a lower power mode and a power down, comprising:

a first port that receives data from the host processor via a system bus;

a second port that transmits data to the network;

a memory that stores data packets in transit between the host processor and the network;

a medium interface unit coupled to network media supporting at least a high speed protocol and a lower speed protocol;

~~a voltage detector for detecting power supply voltage on the bus;~~ and

power management logic on the integrated circuit comprising a state machine having a full power state, a low power state, and a power down state, configured to cause ~~which forces~~ the medium interface unit to renegotiate from the high speed protocol to the lower speed protocol in response to an event ~~detected by the voltage detector~~ signaling entry to the lower power mode and to cause the medium interface unit to enter a power down mode if the lower speed protocol is not successfully renegotiated.

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20. (Original) The integrated circuit of claim 19, wherein the first port, second port, memory and medium interface unit when executing said lower speed protocol consume less than a specified power for said lower power mode, and consume greater than the specified power when executing said high speed protocol.

21. (Original) The integrated circuit of claim 19, wherein the first port, second port, memory and medium interface unit when executing said lower speed protocol consume less than a specified power of about 1.3 Watts for said lower power mode, and the consume greater than the specified power when executing said high speed protocol.

22. (Original) The integrated circuit of claim 19, including logic operating in said lower power mode using the lower speed protocol to detect a pattern in incoming packets, and in response to detection of said pattern, to issue a reset signal for a host processor.

23. (Original) The integrated circuit of claim 19, wherein the medium interface unit comprises circuitry for formatting packets according to protocols compliant with 10 Megabit, 100 Megabit and Gigabit Ethernet protocol standards, and wherein said high speed protocol is Gigabit Ethernet, and said lower speed protocol is one of 10 Megabit Ethernet and 100 megabit Ethernet.

24. (Original) The integrated circuit of claim 19, wherein the medium interface unit comprises circuitry for formatting packets according to a protocol compliant with an InfiniBand protocol standard, and wherein said high speed protocol is InfiniBand.

25. (Previously presented) The integrated circuit of claim 19, including logic to generate indications of a wake up event involving a loss of link or a change of link, and wherein said power management logic blocks signals indicating said wake up event for a time interval during which the power management logic forces the medium interface unit to the lower speed protocol.

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26. (Currently amended) The integrated circuit of claim 19, wherein said event ~~detected by the voltage detector~~ signaling entry into the lower power mode is a signal generated by the host processor.

27. (Previously Presented) The integrated circuit of claim 19, wherein said integrated circuit includes power detection circuit adapted for connection to a system power supply, and said event detected by the voltage detector signaling entry into the lower power mode comprises a loss of power from the system power supply.

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